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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,276	12/09/2003	Mark R. Thomann	303.594US2	4965

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
NAMAZI, MEHDI	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,276	THOMANN ET AL.	
	Examiner	Art Unit	
	Mehdi Namazi	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/20/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34 and 44-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-22 and 32-35* is/are allowed.

6)☒ Claim(s) *23-31 and 44-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed December 20, 2004.

Response to Arguments

2. Applicant's arguments with respect to claims 1-35, and 44-76 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 23-30, and 31 are rejected under the judicially created doctrine of double patenting over claim 7 of U. S. Patent No. 6,694,416 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

A question of patentability is raised with respect to representative claims 1-35, and 44-76 of the instant application under the judicially doctrine of "obviousness-type" double patenting with respect to U.S. Patent No. 6,694,416.

More specifically, OPQR maintains that in view of the "obviousness-type" double patenting rational enunciated in Georgia pacific Corp v United States Gypsum Co., 52 USPQ2d 1590, U.S. Court of Appeals Federal Circuit 1999, representative application claims 1-25 merely defines an obvious variation of the invention claimed in US Patent 6,636,950.

Initially it should be noted that the present application is a continuation application of parent patent 6,694,416 having the same inventive entity. The Assignee in both applications is Micron Technology Inc. The entire disclosures of the instant application and patent number 6,694,416 are identical.

Claim 7 of the patent is compared to claims 23, and 31 of instant application in the table below.

Instant Application	Patent
Claim 23 **An integrated circuit, comprising;** **a first array of memory cells having first data;** **a second array of memory cells having second data;** **a first pipeline operable for outputting data on a rising edge of a clock, the first pipeline having a first data mux**	Claim 7. **An integrated circuit comprising:** **A first array of memory cell having first data;** **A second array of memory cell having second data;** **A first pipeline, having a first data mux connected to the first array and a first latch, and operable for outputting data**

connected to the first array and a first latch', **a second pipeline, in parallel with the first pipeline, operable for outputting data on a** **falling edge of the clock, the second pipeline having a second data mux connected to the second array and a second latch;** **a data mux controller connected to the first and second data muxes to direct the first data to the first pipeline ;** and to direct the second data to the second pipeline; wherein the first data mux is further connected to the second array; and an output buffer connected to the first and second pipeline.	**on a rising edge of a clock;** **a second pipeline, in parallel with the first pipeline, having a second data mux connected to the second array and a second latch, and operable for outputting data on a falling edge of the clock; and** **a data mux controller connected to the first pipeline and to direct the second data to the first pipeline.**
Claim 31 **An integrated circuit comprising:** **a first memory array;** **a second memory array;**	Claim 7. **An integrated circuit comprising:** **A first array of memory cell having first data;** **A second array of memory cell having**

	second data;
a first pipeline, having a first data mux connected to the first memory array and the second memory array, for outputting data on a rising edge of a clock;	**A first pipeline, having a first data mux connected to the first array and a first latch, and operable for outputting data on a rising edge of a clock;**
a second pipeline, having a second data mux connected to the first memory array and the second memory array, for outputting data on a falling edge of the clock; and	**a second pipeline, in parallel with the first pipeline, having a second data mux connected to the second array and a second latch, and operable for outputting data on a falling edge of the clock; and**
a data mux controller connected to the first and second data muxes to direct data from the first memory array and the second memory array to the first pipeline and the second pipeline.	**a data mux controller connected to the first pipeline and to direct the second data to the first pipeline.**

Claims 23-30, and 31 of the instant application are anticipated by claim 7 of that patent. Claims 23-30, and 31 of the instant application therefore are not patently distinct from the earlier patent claims and as such is unpatentable for obvious-type double patenting.

Under the rules of GATT/NAFTA for implementation of the 20 years term effective June 8, 1995, the term of the affronted U.S. patent ends the same date as the instant application. Therefore, patent protection rights due application from U.S. Patent No. 6,694,416 B1 cannot be timewise extended by issuance of the instant application even without a properly drafted terminal disclaimer in this case. **However in lieu of the cancellation of the claims or abandonment of the instant application, applicants must overcome this question of patentability by submission of a paper that at least addresses the "enforceability/common ownership" provision of a terminal disclaimer referred to in 37 CFR 1.321 (C) (3).**

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 44-70 are rejected under 35 U.S.C. 102(B) as being anticipated by IBM (Technical Disclosure Bulletin vol. 30 no. 12 May 1988).

As per claims 44, 58, 64, IBM teaches a method for reading data on a memory device having a storage unit (RAM A, and RAM B) , a first pipeline (fig. 1, element 13), a second pipeline (fig. 1, element 14), and an output buffer (fig. 1, element 21), comprising:

selecting data in a storage unit (counter 15 selects the data);

determining which of the first or second pipeline data is to be placed on (pipeline is selected based on which RAM has been clocked);

passing the data to the determined pipeline page 339, paragraph 3, lines 6-8); and

passing data from the pipeline to the output buffer (page 339, paragraph 3, lines 10-11, data is passed through a multiplexer into DAC which is consider as buffer).

As per claim 45, IBM teaches wherein determining includes selecting a pipeline that can output data on rising edges of an external clock (page 339, paragraph 3, lines 5-8).

As per claim 46, IBM teaches wherein determining includes selecting a pipeline that can output data on falling edges of an external clock (page 341 paragraph 1, the data is outputted from each rising or falling edge).

As per claims 47, 50, IBM teaches wherein the determining includes determining based on the address of the data (the determination is based on which RAM hold the data).

As per claims 48, 51, IBM teaches wherein the determining includes determining based on latency of data (page 341, paragraph 1).

As per claims 49, 52, IBM teaches wherein the determining includes determining based on a combination of the address of the data and the latency of the data (page 341, paragraph 1).

As per claim 53, IBM teaches a method for reading data on a memory device having a storage unit, a first pipeline, a second pipeline, and an output buffer (fig. 1) comprising:

first determining which of the first or second pipeline a first piece of data is to be placed on (page 339, paragraph 3); first passing a first piece of data from the storage unit to the first determined pipeline (with signal from clock generator 16, data will be send through one of the pipelines 13 or 14, based on where the data is); second determining which of the first or second pipeline a second piece of data is to be placed on data is sent out (page 340, paragraph 1, lines 5-8); second passing a second piece of data from the storage unit to the second determined pipeline (page 340, lines 5-8)'; further determining which of the first or second pipeline further pieces of data are to be placed on (page 339, paragraph 3); further passing pieces of data from the storage unit to the further determined pipeline (page 339, paragraph 3, lines 6-8); and passing data to the output buffer from the pipeline (page 339, paragraph 3, lines 6-11).

As per claim 54, IBM teaches wherein the first passing and the second passing occur simultaneously (page 340, lines 6-8; by Simultaneously clocking RAM A, and RAM B).

As per claim 55, IBM teaches wherein the first passing and the second passing occur alternatingly (by alternatively clocking RAM A, and RAM B).

As per claim 56, IBM teaches passing occurs simultaneously with additional passing of pieces of data (by Simultaneously clocking RAM A, and RAM B).

As per claim 57, IBM teaches wherein further passing occurs altematingly with additional passing of pieces of data (by alternatively clocking RAM A, and RAM B).

As per claim 59, IBM teaches the timing is such that data passed from the pipelines to the output buffer can be read on rising and falling edges of an external clock (page 341, paragraph 1).

As per claim 60, IBM teaches the timing is adjusted based on cycle time (page 340, lines 1-5).

As per claim 6l, IBM teaches the timing is adjusted based on latency (page 341, lines 1-4).

As per claim 62, IBM teaches the timing is adjusted based on some combination of cycle time and latency (pages 340, first paragraph, 341 paragraph 1).

As per claim 63, IBM teaches the timing is set such that data can be read on a first and second event (page 340, switching between RAM A, and RAM B consider as first and second event).

As per claim 65, IBM teaches the read command is a processor request to read the data of a certain memory location (it is inherent to read data from certain memory based on processor request).

As per claim 66, IBM teaches the certain memory location is a storage unit (RAM A, and RAM B).

As per claim 67, IBM teaches certain memory location is an array (fig. 1, elements 10, and 11).

As per claims 68, 70, IBM teaches certain memory location is a memory device (fig. 1, elements 10, and 11).

As per claim 69, IBM the system device is a processor(system will not work without processor).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 71-76 are rejected under 35 U.S.C. 102(e) as being anticipated by Li (US. 6,446,180).

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 71, Li teaches a method of reading data, comprising issuing a read command (col. 4, lines 46-61); selecting from a plurality of pipelines (col. 4, lines 46-61) first passing a piece of data from a certain memory location to a strobe

latch of the selected pipeline (fig. 2, element 130), second passing the piece of data from the strobe latch of the selected pipeline to the delay latch of the selected pipeline (fig. 2, element 135); and third passing the piece of data from the delay latch of the selected pipeline to a system device (fig. 2, element 140).

As per claim 72, Li teaches the second passing occurs on an edge of an external clock (col. 4, lines 46-61).

As per claim 73, Li teaches the second passing occurs on an event or signal other then an edge of an external clock (col. 4, lines 46-60).

As per claim 74, Li teaches the third passing occurs on an edge of an external clock (col. 4, lines 46-61).

As per claim 75, Li teaches the third passing occurs on an edge of a clock in advance of an external clock (col. 4, lines 46-61).

As per claim 76, Li teaches the first, second and third passing occur based on a DLL clock (col. 1, lines 55-65).

Allowable Subject Matter

6. Claims 1-22, 32-35 are allowed.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 571-272-4209. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
3/21/05

Mehdi Namazi
March 21, 2005

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER